CT-Bus : A Heterogeneous CDMA/TDMA Bus for Future SOC

Bo-Cheng Charles Lai[1] Patrick Schaumont[1] Ingrid Verbauwhede[1,2]
[1]UCLA, EE Dept. [2]K.U.Leuven
420 Westwood Plaza
Los Angeles, CA 90095

Abstract- **CDMA interconnect is a new interconnect mechanism for future SoC. Compared to a conventional TDMA-based bus, a CDMA-based bus has better channel isolation and channel continuity. We introduce a new bus architecture called CT-Bus, which mixes and takes strengths of both CDMA-based and TDMA-based interconnect schemes. A CT-Bus gives designers the ability to cope with widely varying communication requirements. We propose a method and a tool to explore the mapping of heterogeneous traffic flows onto the CT-Bus. Simulation results on a multimedia mobile phone system show that traffic flows mapped onto a CT-Bus meet the latency requirements while the same traffic flows mapped onto a conventional TDMA-only bus violate these requirements.**

1. INTRODUCTION

The future SOC (system on a chip) will consist of a heterogeneous mix of components and functional units that are tailored towards the specific application domain. For instance, a multimedia mobile phone requires dedicated RF and base-band components for wireless communication, DSP engines for real-time signal processing applications, video sensors to take image data, co-processors or accelerator units for video and image processing (Fig.1). However, communication among different IP-cores (intellectual-property) on chip has become one of the major bottlenecks for future SOC [1]. The patterns and behavior of traffic flows among these cores are heterogeneous, in terms of different data rates, bursty or regular, periodic or sporadic, etc. Different performance requirements, e.g. latency of packets, are posed on different types of traffic flows. The communication architecture for SOC should be able to transport the heterogeneous traffic efficiently while still maintaining the required performance. There is no standard solution as to establishing a fast, flexible, efficient and easy-to-design communication network to connect a large number of IP cores that have heterogeneous requirements.

Current techniques to reuse the scarce interconnection resources at the physical level can be categorized into several schemes, time-division, code-division and frequency-division, etc[2]. In this paper, we focus on time-division and code-division schemes. In a time-division scheme, the interconnect resources are shared in the time domain. Arbitration and control of the interconnects are also made based on timing information of the communication modules. In contract to the time-division schemes, code division schemes expend the resources in the code-space domain, while control of the channel access is also being made on code-space domain. Most of interconnect networks in modern SOC rely on busses, which apply time-division multiple access (TDMA) to reuse expensive on-chip wires, e.g. the AMBA bus [4]. Code-division multiple access (CDMA) has recently been proposed as a new interconnect mechanism for next generation systems [3].

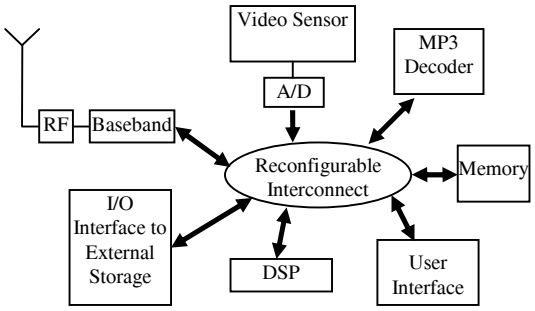

Fig.1: Mobile phone system composed of heterogeneous cores

In this paper, we introduce a new bus architecture, CT-Bus, which mixes and takes strengths of both CDMA-based and TDMA-based interconnect schemes. Performance degradation due to the impact from different types of traffic flows will be alleviated by using CT-Bus. We also introduce a design framework, CT-Sim, which can easily explore the communication mapping of heterogeneous traffic flows onto a CT-Bus. By using the design of the communication architecture of a multimedia mobile phone, we demonstrate how to allocate the heterogeneous traffic flows of the system onto a CT-Bus.

0-7803-8622-1/04/$20.00 ©2004 IEEE

Section 2 briefly introduces the CDMA interconnect and proposes a new bus architecture, CT-Bus. Section 3 proposes a design framework, CT-Sim, to explore the design of the communication mapping onto CT-Bus. A multimedia mobile phone system will be used as one example to demonstrate the benefits of CT-Bus in section 4. Section 5 introduces some related works on CDMA interconnect and discusses the fundamental differences between CDMA and TDMA-based bus. The conclusion will be drawn in section 6.

2. CDMA-TDMA MIXED MODE BUS

From the bus communication point of view, code-division schemes of interconnect have better features on channel isolation and channel continuity. Status-based arbitration flow of the code-division scheme also makes the control of the bus very different from the conventional time-division type of bus. CDMA has recently been used as an alternative to reuse the interconnect resources on chip [3].

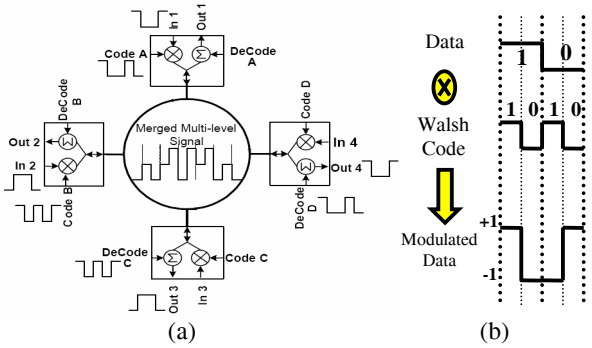

Fig.2 : (a) CDMA-based interconnect (b) Modulation of data and spreading code [3]

2.1. CDMA Interconnect

CDMA is a spread-spectrum technique that allows simultaneous use of the communication medium by multiple information links [5]. It relies on the principle of codeword-orthogonality, that avoids cross-correlation of codewords and allows perfect separation of information modulated with different codewords. Fig.2(a) shows the basic idea of CDMA-based interconnect. Prior to transmitting the data onto the channel, each user modulates each transmitted bit with a spreading code. The spreading code expands the transmission time from a single symbol into multiple chip periods. On the channel, multiple transmissions can coexist as a multi-level signal. At the receiver, this signal is correlated with the same spreading code that was applied at one of the transmitters. Because spreading codes are orthogonal, the original symbol that is transmitted by the transmitter can be retrieved. Fig.2(b) gives an example of a widely-used spreading code, the Walsh-Hadamard code[5]. In a channel with 2 concurrent CDMA links, a 2-bit Walsh code is used and a data bit will be expanded into two chips. Two clock cycles are needed to receive one bit of data if the receiver can receive one chip per clock cycle.

2.2. CDMA-TDMA Mixed Mode Bus (CT-Bus)

Here we propose a mixed-mode bus architecture, CT-Bus, which integrates both CDMA and TDMA techniques in a hierarchical structure (Fig.3), and benefit from both of them. A CT-Bus supports a fixed amount of CDMA *sub-channels* that are separated by different spreading codes. Two or several sub-channels can be grouped as one *sub-channel group*. As shown in Fig.3, there are six CDMA sub-channels in the CT-Bus, and are divided into three different sub-channel groups. The DF1 to DF4 illustrate data flows that need to be assigned to different sub-channel groups. Because of the channel isolation feature of CDMA scheme, data flows on different sub-channel groups will be well isolated without having impact on each other. For each CDMA sub-channel-group, the data flows are further assigned to different TDMA time slots.

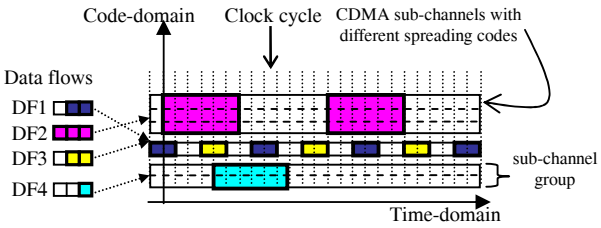

Fig.3: Architecture of CT-Bus (with three CDMA sub-channel-groups)

Reallocation of the traffic flows to sub-channel groups can be achieved by simply re-assigning the spreading codes to traffic flows. Therefore, CT-Bus can be easily reconfigured towards the demands of the system.

3. CT-SIM AND DESIGN EXPLORATION

3.1. CT-Bus Simulation Tool (CT-Sim)

A simulation platform, CT-Sim, has been developed to simulate and analyze the performance of a CT-Bus. CT-Sim is based on the PARSEC language[6]. By using CT-Sim, the architecture of a specific CT-Bus can be easily configured and simulated by setting the configuration parameters. CT-Sim will generate the specific simulation framework based on the configuration parameters. Simulation of a CT-Bus will be run and the results of the system performance will be collected automatically. Designers can explore the design space and make decision based on the results.

As shown in Fig.4, the configuration of CT-Sim simulator has three distinct inputs: the architecture of a CT-Bus, properties of the traffic flows and a mapping of traffic flows. The parameters in a CT-Bus architecture that need to be

decided are the general setting of the bus interconnect, such as total bandwidth of the bus and the number of CDMA sub-channels that are supported in the CT-Bus. Three kinds of

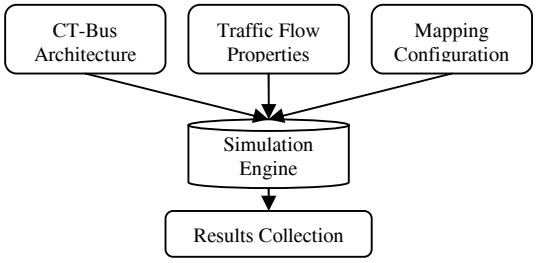

Fig.4: Flow of CT-Bus Simulator

arbitration policies, round-robin (RR), fixed-priority (FP), and weight-fair-queuing (WFQ) can be chosen and assigned to each sub-channel group. In fixed-priority arbiter, the transmitter with the highest priority gets the access to the bus. Round-robin gives each transmitter the right to access the bus in turn. WFQ differs from round-robin in that each transmitter can receive a differential amount of service in an interval of time based on the weight factors of transmitters. The characteristics of each traffic flow are defined in the traffic flow property section. The mapping configuration and the priority of each traffic flow onto the CT-Bus are specified in the mapping configuration section. Table 1 lists the parameters that can be configured in each configuration section.

Table 1: Configuration parameters of CT-Sim

Configuration Section	Parameters
CT-Bus Architecture	– Bandwidth of the CT-Bus – Number of CDMA sub-channels – Number of CDMA sub-channel groups – Arbitration policies for each sub-channel group (RR, FP, or WFQ)
Traffic Flow Properties	– Number of traffic flows – Type and properties of each traffic flow (e.g. type:periodic-regular, data rate: 64Kb/s, etc)
Mapping Configuration	– Which traffic flow is mapped to which sub-channel group

3.2. Design Exploration

Our exploration flow consists of finding a way to group traffic flows and allocate groups onto the CT-Bus (Fig.5). The goal is to meet the requirements of the traffic flows. The exploration flow of communications on CT-Bus can be formulated as follows:

– *Step1: Group traffic flows.* We assumed that before entering the exploration flow, the designer has the properties of each data flow. Traffic flows will be categorized and grouped in this step. The traffic flows in the same group should have minimum impact on each other. The grouping strategies will be discussed in section 3.2.

– *Step2: Map traffic groups onto a CT-Bus*. Based on the requirement of the bandwidth, each group will be mapped onto CT-Bus with appropriate amount of CDMA sub-channels.

– *Step3: Decide arbitration policies*. Given different features and requirements in the group, appropriate arbitration policies will be chosen and assigned to the group.

After step3, a candidate mapping configuration is generated. The configuration parameters will be input into the CT-Sim and a detailed performance of the candidate solution will be generated and analyzed. Designers can use the results of CT-Sim to decide whether to use this candidate configuration or go back to step1 and keep refining the system.

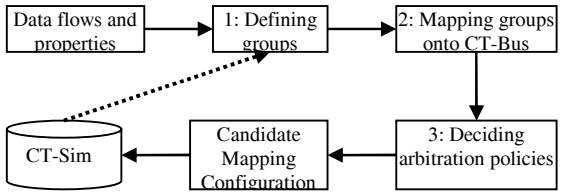

Fig.5: Design and exploration flow of CT-Bus

4. A CASE STUDY: MULTIMEDIA MOBILE PHONE SYSTEM

As illustrated in section 1, in order to achieve energy efficiency and required performance, a multimedia mobile phone system consists of application specific computation cores with heterogeneous traffic flows among them (Fig.1). In this section, we demonstrate the design of the communication architecture of a multimedia mobile phone system. Fig.6 shows the traffic flows among different cores in the system. Table 2 specifies the characteristics of each traffic flow.

All the cores are connected through a CT-Bus. The CT-Bus has a total bus bandwidth of *2Mb/s*, supporting four CDMA sub-channels, such that each CDMA sub-channel has a bandwidth of 512kb/s. In order to give a better understanding of the benefits of CT-Bus, we simplify the problem and assume that each core in the system operates fast enough to send/receive the data flows without additional overhead. The mapping configuration is shown in Table 3. For comparison, the same set of traffic flows is also mapped onto a 2Mb/s TDMA-only bus, which uses fixed-priority arbitration policy.

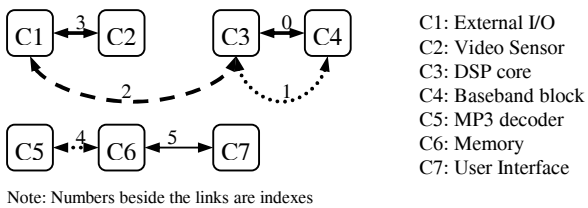

Fig 6: Traffic flows of a multimedia mobile phone

Table 2: Characteristics of traffic flows on a multimedia mobile phone system

Traffic flows	Type	Between cores	Rate/ Burst size	Latency Requirement	Remark
0	p-b	C3-C4	1 kb/s	LS: 0.0001 sec	DSP synchronization data with baseband core
1	p-r	C3-C4	384 kb/s	LS: 0.1 sec	Signals from baseband to DSP (data rate of 3G mobile phone)
2	s-b	C1-C3	312 kb	LS: 0.15 sec	DSP reads a real-time file from external storage element
3	p-b	C1-C2	594 kb/s	LS: 0.15 sec	Video data from video-sensor to UI display (CIFF format, 3 frames/s)
4	p-r	C5-C6	64 kb/s	LS: 0.15 sec	MP3 reads a music file from memory
5	s-r	C6-C7	48 kb	Don't care	UI (microphone) sends voice record to be saved in memory

Note: In the column of Type, "p" is "periodic", "s" is "sporadic", "r" is "regular", "b" is "bursty". In the column of Requirement, "LS" means "Latency Sensitive", data latency cannot be larger than the amount of time specified in this column.

Table 3: Mapping configurations

	CDMA sub-channel group	# of CDMA sub-channels	Arbitration policy	Data flows (DF) assigned to this group
CT-Bus	0	1 (512kb/s)	WFQ	1,4
	1	2 (1Mb/s)	FP	0,3,5
	2	1 (512kb/s)	FP	2
TDMA		2Mb/s	FP	0,1,2,3,4,5

Note : The priorities of data flows are in the descending order from left to right, e.g. in TDMA, flow 0 has higher priority than flow 1.

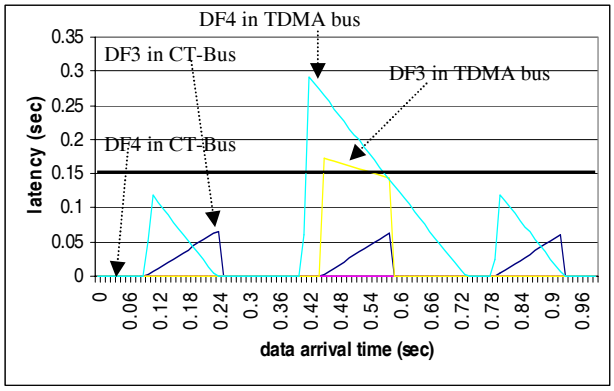

Fig.7: Latencies of traffic flows

Fig.7 shows the simulation of latencies of data flow 3 and 4 (DF3, DF4) for a period of one second. In the CT-Bus, DF4 is assigned in the same sub-channel group as DF1, which is also a periodic-regular data flow. Thus the maximum latency for DF4 is only 33 cycles. Although DF3 is a periodic-bursty data flow, the maximum latency in CT-Bus is 0.06sec. Due to the channel isolation feature of CT-Bus, the latencies are very predictable and well controlled under the latency requirement of 0.15sec. In the TDMA-only bus, the latency of bursty DF3 is alleviated because the bandwidth of the TDMA-only bus is higher than the sub-channel group one of the CT-Bus and the priority of DF3 is high enough to occupy the access to the TDMA-only bus. However, in the TDMA-only bus, DF3 is impacted by DF2, which is also a bursty traffic with a high priority happening from 0.4sec to 0.6sec. DF4 has lower priority than DF2 and DF3 in the TDMA-only bus, thus it is influenced by both of DF2 and DF3. The maximum latency of DF3 and DF4 reaches 0.17sec and 0.3sec respectively, which both violate the latency requirements.

5. RELATED WORK OF CDMA INTERCONNECT

5.1. Prior Art on CDMA Interconnect

The binary CDMA bus [7] avoids multi-level signaling representations by encoding the summation. The feasibility of CDMA-based buses has been demonstrated at the physical level. A self-synchronizing CDMA transmitter and receiver has been demonstrated using 2-bit Walsh spreading codes and achieves 2.7 Gbps [8]. A Source-synchronous CDMA bus interface uses an additional clock signal to perform synchronization [9]. It requires less area than [8], and can achieve 2 Gbps. Both [8] and [9] use PAM (Pulse Amplitude Modulation) to realize multi-level signaling of CDMA interconnect. Besides TDMA and CDMA, one can imagine to apply other techniques to reuse the limited on-chip channels, e.g. frequency-division multiple access (FDMA) [3].

5.2. Comparison Between CDMA and TDMA

In this section we enumerate the fundamental differences between CDMA interconnect and the conventional TDMA interconnect.

5.2.1. Channel Isolation

The CDMA interconnect has better channel isolation than TDMA in the time domain. Different sub-channels of CDMA are using different spreading codes and the interferences between channels can be compensated at the receiver side. Therefore, we can simply consider each sub-channel of CDMA as an independent channel which is separated by different spreading codes.

5.2.2. Channel Continuity

The TDMA-based bus divides the channel in the time domain and chops the channel granularity into time slot

periods. This basic unit cannot easily be changed. The disadvantage of this discontinuity in the channel can be easily demonstrated when the packets need to be fragmented after packet size has been changed. The CDMA-based bus has better channel continuity in time domain since the channel is divided by the spreading-codes.

5.2.3. Channel Granularity (Scalability)

Channel granularity decides how accurate and how fair the arbitrator can assign sub-channels to different transmitters. For example, given data stream A and B with data rates of 4KB/s and 5KB/s respectively, the arbitrator of TDMA bus can give 4 time slots to A and 5 time slots to B within a 9 time-slot period. For a CDMA interconnect, this fine granularity is more difficult to achieve because CDMA bus can only support a fixed amount of sub-channels.

5.2.4. Arbitration Flow

The arbitration mechanisms of TDMA and CDMA schemes solve problems from different points of view, in time domain and code-space domain respectively. We categorize the arbitration mechanism of a TDMA bus and a CDMA bus as *time-based* and *status-based* respectively. The network connectivity of TDMA is decided by the activation of a "GRANT" signal given by the arbiter at every time period while CDMA is determined by spreading codes that are being used (Fig.8). This implies that the arbiter of a TDMA bus needs to take care of all the control signals and switching behavior at every time slot period. However, the arbiter of CDMA bus only needs to manage and assign spreading codes to modules whenever the reconfiguration status of the system has been changed, e.g. a transmitter needs to increase the average data rate.

(TDMA Arbitration Flow)

```
While ( every cycle ) {
  If( Status is changed )
     Generate New Schedule ;

  Active "Grant Signal" of
  Modules based on the
  Schedule ;
}
```

(a)

(CDMA Arbitration Flow)

```
While ( Status is changed ) {
  Generate New Schedule ;
  Assign Spreading codes to
  Modules ;
}
```

(b)

Fig.8: Pseudo code of arbitration flow. (a) Time-based bus (b) Spatial-based bus

6. CONCLUSION

In this paper, we introduce a new bus architecture called CT-Bus, which mixes and takes strengths of both CDMA-based and TDMA-based interconnect schemes. With better channel isolation and granularity, a CT-Bus gives designers the ability to cope with widely varying communication requirements. Reconfiguration of CT-Bus can be achieved by simply re-assigning the spreading codes. We propose a method and a tool, CT-Sim, to explore the mapping of heterogeneous traffic flows onto the CT-Bus. The future SOC requires the communication architecture to be able to handle heterogeneous traffic flows. Simulation results on a multimedia mobile phone system show that CT-Bus can handle the heterogeneous traffic flows very well and meet the latency requirements.

7. ACKNOWLEDGEMENT

The authors would like to thank Jongsun Kim and Prof. Frank Chang for the interesting discussions. They acknowledge the support from NSF CCR-0310527, from SRC 2003-HJ-1116, and from UC-Micro 02-079 and 03-088.

8. REFERENCES

[1] M.Sgroi, and et al., "Addressing the System-on-a-Chip Interconnect Woes Through Communication-Based Design," DAC, June, 2001

[2] I. Verbauwhede and M.-C. F. Chang, "Reconfigurable interconnect for next generation systems," SLIP, pp. 71-74, April 2002.

[3] M.Frank Chang, and et al., "RF/Wireless Interconnect for Inter- and Intra-chip Communications," Proceedings of the IEEE, vol.89, no.4, pp.456-466, 2001.

[4] Advance Microcontroller bus Architecture (AMBA). http://www.arm.com/ .

[5] J.S.Lee, L.E.Miller, "CDMA Systems Engineering Handbook," Artech House Publish, 1998. ISBN: 0-89006-990-5

[6] UCLA Parallel Computing Laboratory: Parallel Simulation Environment for Complex Systems (PARSEC). http://pcl.cs.ucla.edu/projects/parsec/

[7] R. H. Bell, C. Y. Kang, L. John, E. E. Swartzlander: CDMA as a Multiprocessor Interconnect Strategy. Thirty-Fifth Annual Asilomar Conference on Signals, Systems and Computers, pp.1246-1250, Nov 2001.

[8] Z. Xu, and et al., "A 2.7 Gb/s CDMA-interconnect Transceiver Chip Set with Multi-level Signal Data Recovery for Reconfigurable VLSI Systems," ISSCC, vol.1, pp. 82-83, February 2003.

[9] J. Kim, Z. Xu, and M.F. Chang, "A 2-Gb/s/pin Source Synchronous CDMA Bus Interface with Simultaneous Multi-Chip Access and Reconfigurable I/O Capability," CICC, pp. 317-320, Sept. 2003.