Erratum to the paper:
Embedded Software Integration for Coarse-grain Reconfigurable Systems

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Table 2 in the paper compares the performance improvement obtained by hardware acceleration of a software algorithm. Three algorithms are considered: Discrete Fourier Transform (DFT), Advanced Encryption Standard (AES) and TCP/IP Checksum Evaluation. Each algorithm uses a different style of hardware acceleration, using a register-mapped coprocessing architecture for DFT, a memory-mapped coprocessing architectures for AES, and a network-mapped coprocessing architecture for Checksum. The methodology of measurement consists of comparing a software-only version of the algorithm to a hardware-accelerated version. For each testcase, both the execution runtime as well as a power consumption estimate are obtained. The energy consumption is obtained by multiplying the power consumption estimate with the execution runtime of the algorithm. Comparing the energy consumption of the software implementation to the hardware-accelerated case, we obtain the energy-efficiency improvement.

The execution time of the software implementation of the checksum algorithm as published in Table 2 of the paper contains an error. The correct execution time is shown in Table 1 below. This is the execution time of the software without compiler optimization. The resulting energy-efficiency improvement changes as well. Of course, it must be kept in mind that these numbers are estimates, not actual measurements. The key point of the Table is to illustrate that distributed architectures can achieve better energy-efficiencies than centralized architectures. This conclusion remains valid with the new figures.

Table 1: Design results for the three design cases. The shaded cells contain corrections.

Application	Target Architecture	Performance (ms)	Implementation Cost (Memory + LUT)	Estimated Power (mW/MHz)	Estimated Energy (mJ)
DFT (1000 iterations)	SW on LEON2	118.7	9.7 KByte ROM 4856 LUT	11.4	67.6
	LEON2 with Accelerator HW	9.23	8.9 KByte ROM 7700 LUT	12.5	5.76 **(12X Improvement)**
AES (175 iterations)	SW on LEON2	158.3	36.3 KBytes ROM 4856 LUT	11.4	89.2
	LEON2 with Accelerator HW	5.23	8.6 KByte ROM 8330 LUT	13.5	3.5 **(25X Improvement)**
TCP/IP Chksm (100 packets from HTTP seq)	SW on LEON2	**23.20**	10.0 KByte ROM 4856 LUT	11.4	**13.2 (66X Improvement)**
	Accelerator HW (stand-alone *)	0.699	1556 LUT	5.78	0.20

(*) The implementation and performance is that from a stand-alone checksum verifier/inserter