A 5.6-mW 1-Gb/s/pair Pulsed Signaling Transceiver for a Fully AC Coupled Bus

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***Abstract*—This paper describes a low-power synchronous pulsed signaling scheme on a fully ac coupled multidrop bus for board-level chip-to-chip communications. The proposed differential pulsed signaling transceiver achieves a data rate of 1 Gb/s/pair over a 10-cm FR4 printed circuit board, which dissipates only 2.9 mW (2.9 pJ/bit) for the driver and channel termination and 2.7 mW for the receiver pre-amplifier at 500 MHz. The fully ac coupled multipoint bus topology with high signal integrity is proposed that minimizes the effect of inter-symbol interference (ISI) and achieves a 3 dB corner frequency of 3.2 GHz for an 8-drop PCB trace. The prototype transceiver chip is implemented in a 0.10-μm 1.8-V CMOS DRAM technology and packaged in a WBGA. It occupies an active area of 330×85 μm^2.**

***Index Terms*—AC coupled bus, chip-to-chip communication, I/O interface, multipoint bus, pulsed signaling, transceiver.**

I. Introduction

TECHNOLOGY scaling in CMOS chips has increased the internal clock frequency over a few tens of gigahertz, however, the off-chip I/O signaling speed has been scaling much more slowly. Although the CMOS high-speed serial links already entered multi-Gb/s/pin speeds by using point-to-point connections and complicated equalization techniques [1], the speed of a parallel multidrop or multipoint bus (e.g., memory interfaces) is still in less than 2 Gb/s/pin due to the signal integrity issues in a bandwidth-limited printed circuit board (PCB) environment [2]. Also, the signaling power consumption is of increasing concern. The ever-increasing demand for higher aggregate traffic rates will result in over 1 Tb/s/chip in the near future, which may consume over a few tens of watts for only signaling [3], [4]. Integrating a large number of high-speed I/Os on a single chip becomes extremely challenging due to excessive complexity and power consumption.

In conventional bus-based systems with directly coupled multipoint connections, the available channel bandwidth has been primarily limited by the ISI resulting from the impedance discontinuities created by the transmission line stubs and multiple device capacitive loadings. To increase the data rate further, the trend is to replace the system bus with high-speed point-to-point I/O links [5]. However, widely parallel serial links have overhead in terms of large area, cost, and difficulty in system scaling. Therefore, the shared bus architecture is still very attractive for low-latency, high-density and compact size board-level chip-to-chip communications with flexibility. In order to use this parallel bus topology for one more decade or even more, the problem remains how to increase the available bandwidth of a multipoint bus, how to achieve high signal integrity, and how to decrease the signaling power.

To mitigate the effect of ISI, equalization schemes [1] have been applied in directly coupled multipoint bus applications such as memory-to-processor and DRAM controller-to-DRAMs [6], [7]. However, [6] requires the ISI subtraction time, which increases the receiver latency and limits the data rate. A feed-forward equalizer [7] increases the I/O input capacitance, which may degrade the channel characteristics. Thus, these receiver equalization schemes are not simple and cost-effective for multi-Gb/s parallel bus I/Os.

Recently, instead of using a directly coupled bus topology which creates huge aggregate capacitance loadings on a shared line, an electromagnetically coupled memory bus was proposed to remove the connector stubs by using 1-cm zig-zag couplers [8]. Similarly, wireless ac coupling has been applied in proximity point-to-point communication for multichip modules (MCMs) and stacked face-to-face chips to replace the conductive mechanical junction path and increase the density of interconnections [9]–[11]. However, [8] consumes large I/O power of 40 mW/pair, since the motherboard bus is driven by conventional full-swing signaling and [9]–[11] can only be applied to extremely short point-to-point connections. Therefore, these are unsuitable for use in high-speed parallel multipoint bus communications that require lowest I/O power dissipation.

In this paper, we introduce novel circuit techniques [12] that reduce the I/O signaling power by a factor of 7.5 and increase the available channel bandwidth of a multipoint bus by a factor of 2 compared to the most recent memory bus I/O schemes. The demonstration chip, which incorporates differential bidirectional pulsed signaling, achieves 1 Gb/s over 10-cm printed circuit board traces with 2.9 mW of power for the driver and channel termination and 2.7 mW for the receiver pre-amplifier. To achieve this low power and high signal integrity in a multipoint bus, the prototype chip employs two key circuit techniques. First, the pulsed signaling transceiver reduces the I/O power by treating the dc value of signals as redundant and using a diamond data eye. Second, capacitive coupling using on-chip metal–insulator–metal (MIM) capacitors enables a fully ac coupled multipoint bus, which minimizes the impedance discontinuities of a shared bus as well as ISI. This I/O scheme uses conventional packaging and board technologies, which is suitable for low-cost high-density front-side buses or memory buses.

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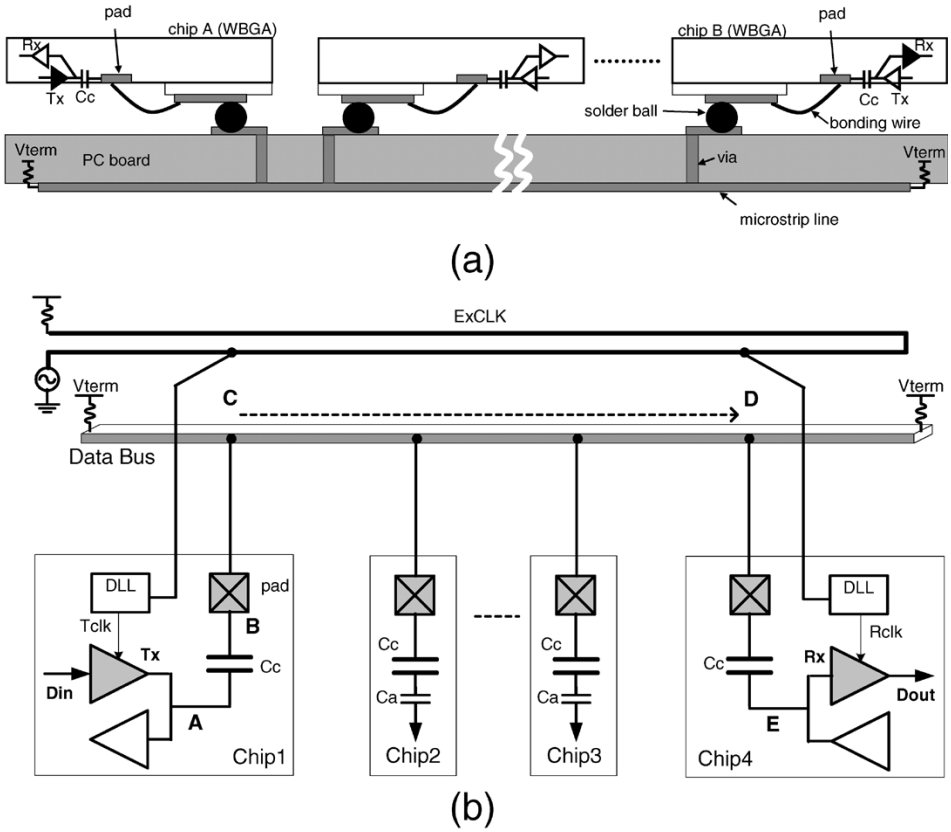


Fig. 1. Pulsed signaling on a fully ac coupled multipoint bus. (a) Board-level structure. (b) Detailed synchronous CCBI system architecture.

This paper is organized as follows. The proposed capacitive coupled pulsed signaling bus interface (CCBI) system architecture and interconnect modeling are described first in Section II. Detailed transceiver circuits, synchronous timing diagram, and simulation results are discussed in Section III. Signal integrity and channel power dissipation are compared with current technologies in Sections IV and V, respectively. Measurement results are given in Section VI.

II. CCBI System Architecture and Interconnect Modeling

The board-level structure of the proposed pulsed signaling system [12] is shown in Fig. 1(a). The chip scale packages (CSPs) such as wirebond ball grid array (WBGA) or micro ball grid array (μBGA) are mounted in a chip-on-board fashion on a conventional PC board trace. On-chip MIM capacitor C_C, which is formed between the two metal plates, decouples the driver and receiver circuits from the I/O pad, and therefore enables a reliable fully ac coupled multipoint bus.

Fig. 1(b) depicts the detailed synchronous, multipoint, bi-directional, CCBI system architecture (single-ended for simplicity) with a round trip clock line. The transmitter (Tx of chip1) and the receiver (Rx of chip4) are coupled to the FR4 PCB trace through an on-chip coupling C_C and a pad at points C and D, respectively. Both ends of the data bus are parallel terminated by the impedance matching resistors (Z_o) with termination voltage $V_{\rm term}$. Source synchronous clocking (with one round trip or two forwarded clocks) is used to remove the skew between the clock and the pulse signals.

To ensure reliable pulsed signaling over 1 Gb/s, the multipoint interconnects and device package loading models need to be accurate up to a few gigahertz. The simplified single-ended pulsed signaling bus model on an ac coupled PCB transmission line is shown in Fig. 2(a). Since the loss of the MIM capacitor, the resistance and the inductance of the metal plates, and the parasitic capacitance between the metal and substrate are negligible at all signal frequencies of interest, a lumped capacitance model can be used for C_C. As shown in Fig. 2(b), the equivalent I/O circuit path serves as a differentiating circuit or a single-time-constant high-pass circuit with a transfer function

$$T(\mathrm{s}) = (C_C/C_{\rm eff})\mathrm{s}R_{\rm eff}C_{\rm eff}/(1+\mathrm{s}R_{\rm eff}C_{\rm eff}) \qquad (1)$$

where $C_{\rm eff} = C_C + C_p + C_{\rm pk}$ and a time constant $\tau = R_{\rm eff}C_{\rm eff}$.$C_p$ and $C_{\rm pk}$ are parasitic capacitances for the bonding pad and package pin, respectively. This can be used to analyze and define the pulse signal characteristics (e.g., eye width and amplitude) on the PCB channel. Fig. 2(c) shows the transient response of this equivalent circuit, which generates a diamond data eye. This high-pass circuit transmits the transient part of the input data. However, the dc signal component is blocked. A step input voltage V_A on node A by the full-swing output driver results in a transient on node C, transforming a square wave binary input into a short triangle pulse wave on the channel with polarity and amplitude (V_p) of about

$$V_p = R_{\rm eff}I_c = \alpha Z_o C_C dV_A/dt \qquad (2)$$

where $R_{\rm eff} = Z_o/2 + R_{\rm pk} + 2\pi f L_{\rm pk} = \alpha Z_o, \alpha = 0.6$–$0.7$, and $Z_o = 50\ \Omega$ in the frequency (f) range of 500 MHz to 1 GHz. Here the induced small current $I_c = C_C dV_A/dt$ on the

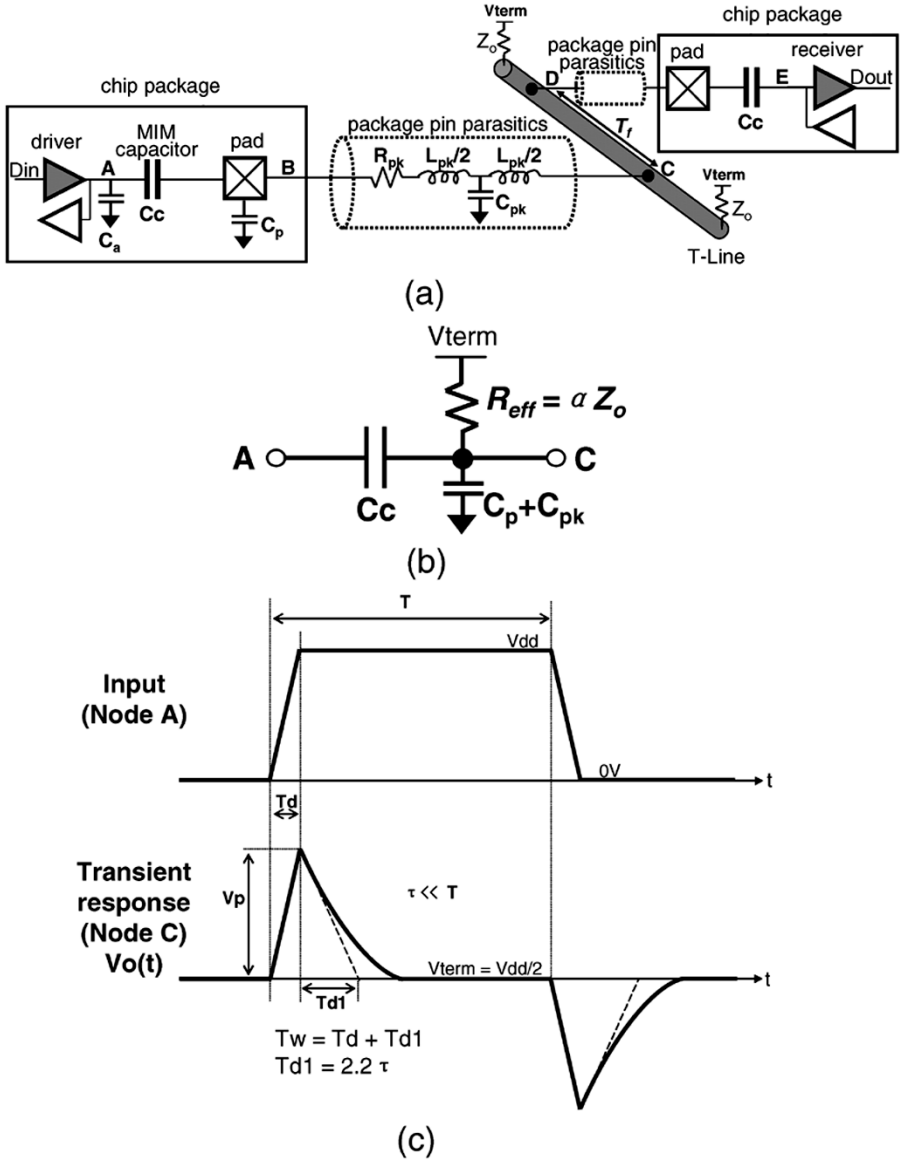


Fig. 2. (a) Modeling of pulsed signaling on an ac coupled PCB transmission line. (b) Equivalent differentiating circuit with a small time constant τ. (c) Transient response of the equivalent circuit with a short triangle pulse.

channel is related to the edge speed $(dt = Td)$ of the driver. The transient output wave form $Vo(t)$ decays exponentially

$$Vo(\mathrm{t}) = V_p \exp(-t/\tau) + V_{\mathrm{term}} \tag{3}$$

toward the termination voltage $V_{\mathrm{term}} = Vdd/2$ with a very small time constant τ

$$\tau = R_{\mathrm{eff}} C_{\mathrm{eff}} = \alpha Z_o (C_C + C_p + C_{\mathrm{pk}}) \tag{4}$$

where C_C is usually 0.5–0.8 pF. If we consider the ESD capacitance (C_{esd}), C_{eff} becomes $C_C + C_p + C_{\mathrm{pk}} + C_{\mathrm{esd}}$, but still τ can be controlled less than 100 ps. It takes rise or fall time of $Td1 = \ln(9)\tau = 2.2\tau$ to get from the 10% to the 90% point. Then the pulsewidth (Tw) on the PCB channel is approximately determined by

$$Tw = Td + Td1 \tag{5}$$

where usually $Td1$ is dominant and $Tw \ll T$. T is the data period. So, the V_p and Tw of the diamond data eye are controlled by choosing the proper values of C_C and $Td1$.

To ensure low energy transmission in this pulsed signaling, the total signal attenuation including PCB channel and package loss need to be analyzed and should be in the range of design tolerance. In Fig. 2(a), the first signal loss occurs through the package pin parasitic of the transmitter output path, from point B to C, including bonding wire, solder bump and via, which is a kind of a band-limiting conductive connection. Similarly at the receiver path, there is package and capacitor loss from point D to E. Low-parasitic chip scale packages employing flip-chip interconnect technology are preferred to minimize this attenuation. However, the dominant signal loss occurs through the multipoint bus and depends on the channel length and the mounted device count. After the propagation delay of T_f, the pulse arrives at the receiver chip with reduced amplitude due to the channel losses (skin effect and dielectric loss), dispersions and reflections on the transmission line. Considering all of these loss factors, channel transfer function simulation results that meet the signaling tolerance requirement are discussed in Section IV. To achieve better noise immunity, by rejecting common-mode dis-

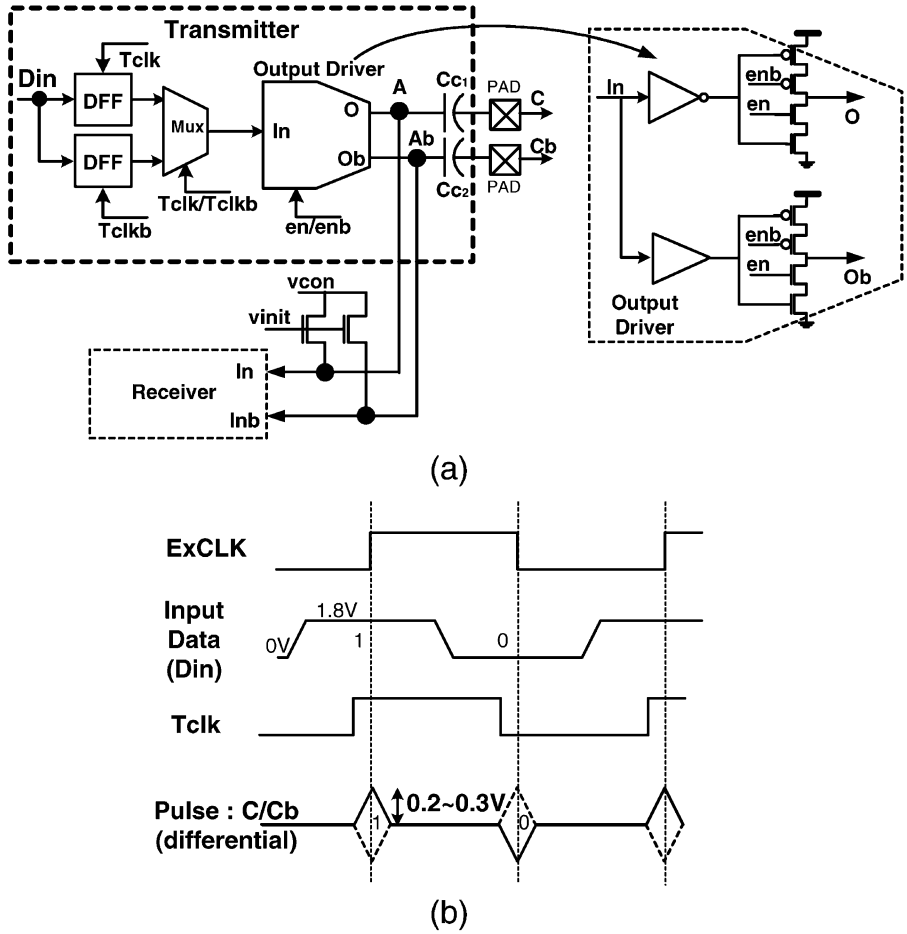


Fig. 3. (a) Transmitter circuit. (b) Transmitter timing diagram of synchronous pulsed signaling.

turbances as well as crosstalk from other noise sources, shielded differential signal lines can be used.

III. CCBI Transceiver Architecture and Timing Diagram

The proposed pulsed signaling transceiver utilizes ac coupling and thus has no dc current component on the channel. It also eliminates the dc balancing problems of the conventional ac coupling schemes [9], [13] without using data encoding or feedback schemes since the transient pulse decays rapidly toward the termination voltage as shown in Fig. 2(c).

Fig. 3(a) shows the transmitter circuit, consisting of D-flip-flops, a multiplexer (mux), and an output driver. The differential output driver consists of small tri-state buffers with full-swing outputs (O/Ob) and a controlled slew rate. When it drives the node A of C_C1, a small current pulse is induced on the other side of C_C1 and converted to a short voltage pulse with polarity and peak amplitude of about 0.2–0.3 V. As shown in the timing diagram of Fig. 3(b), the pulses are synchronized and transferred in parallel with the external clock (ExCLK). This occurs without board level skew by using the Tclk/Tclkb generated from the transmit delay-locked loop (DLL). When the output driver is not active, it is turned off $(\mathrm{en}/\mathrm{enb} = \mathrm{low}/\mathrm{high})$ and A/Ab nodes are precharged and equalized by signal V_{init} to a voltage $V_{\mathrm{con}} = V_{\mathrm{term}}$ to initiate a common-mode. The required size of the output driver to drive the C_C of 0.5–0.8 pF is much smaller than that of the conventional square wave signaling output drivers, resulting in smaller parasitic capacitance C_a at the output node A/Ab and a reduced power dissipation of only 1.3 mW ($C_C V dd^2 f = 0.8$ pF (1.8 V)^2/2 ns) at 500 MHz. Unlike the transmitters of the directly coupled buses consuming both large dc and ac power and introducing large simultaneous switching Ldi/dt noise, this pulsed signaling transmitter consumes only very small ac power. Also, the low-frequency system noise is filtered out by the high-pass transmission characteristic of the ac coupled transmitter path. All of these make it possible for the pulsed signaling transmitter to put less energy into the channel and for the receiver to operate with moderate power dissipation.

Fig. 4(a) shows the receiver circuit, which consists of a differential static pre-amplifier and two typical sense amplifier based flip-flops (SAFFs). Since the incoming signal at node E/Eb is a short pulse with small amplitude, a static cross-coupled pre-amplifier is required to sense and latch it. This differential pre-amplifier, which exhibits hysteresis, has the built-in ability to filter out the incoming noise from imperfect termination and common-mode disturbances such as ground bouncing or power supply drop. The synchronous timing diagram of the receiver is shown in Fig. 4(b). The pulse signal arrives at the receiver in parallel with the ExCLK, and is recovered with a data-to-q delay of $td1$. The center of this data (out/outb) window is phase locked with the Rclk, which is delay compensated $(td2 = td1)$. The 90° shifted clock (Rclk90) is generated from the receive

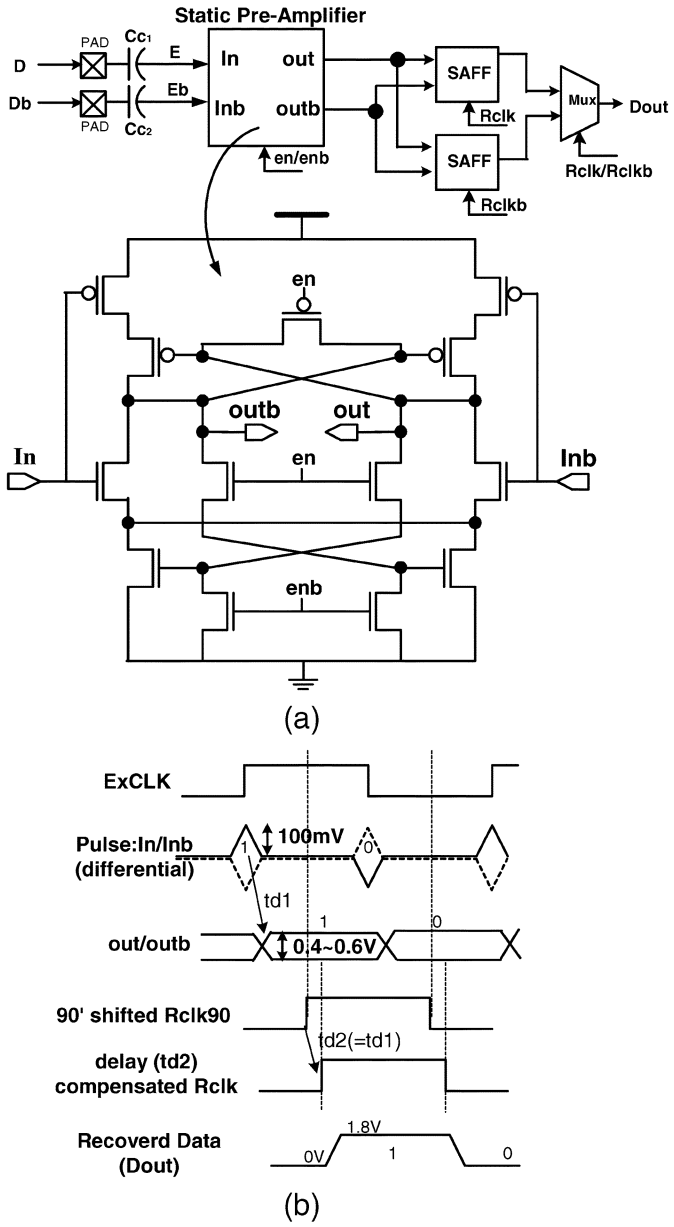


Fig. 4. (a) Receiver circuit with hysteresis. (b) Receiver timing diagram of synchronous pulsed signaling.

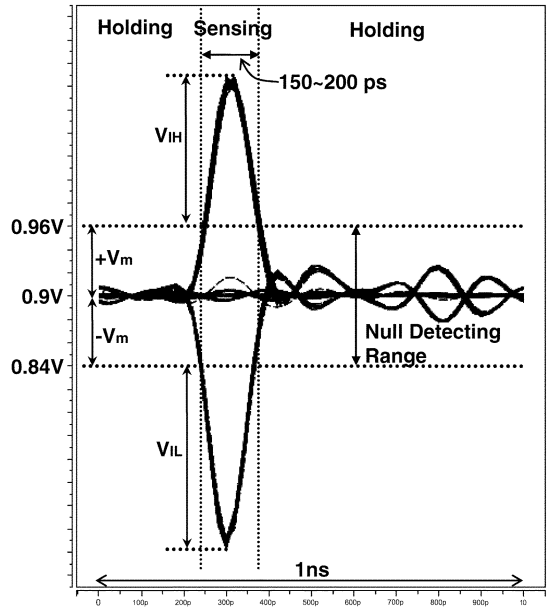


Fig. 5. 1-Gb/s diamond eye diagram at the receiver [pre-amplifier input, point E of Fig. 2(a)] after 10-cm FR4 PCB.

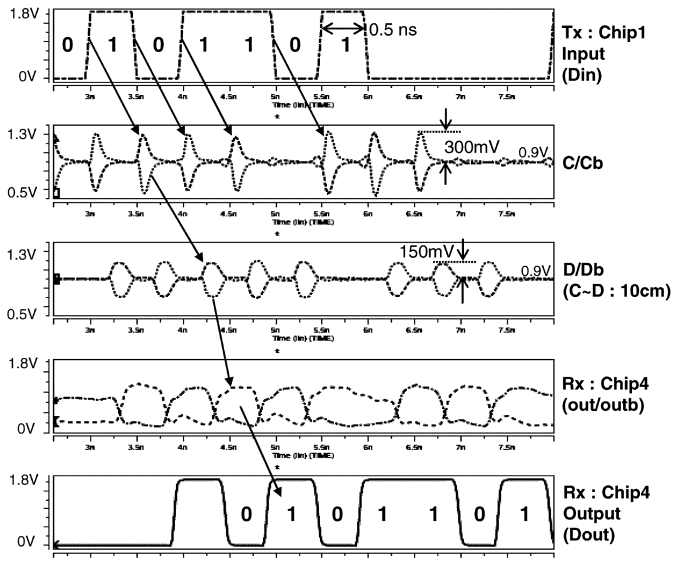


Fig. 6. Simulated 2-Gb/s/pair pulsed signaling over a 10-cm ac coupled 2-drop bus.

DLL by synchronizing with the ExCLK. The differential output (out/outb) is amplified and latched by the demultiplexing SAFFs. The 1-Gb/s differential pre-amplifier operates with a moderate power dissipation of 2.7 mW by sinking a static current of 1.5 mA, which is comparable with that of typical high-speed DRAM receivers with three-stage (pre-amplifier, sense-amp, and latch) structures [16]. The static power can be minimized by switching it off ($\mathrm{en} = \mathrm{low}$) when the receiver is not active.

Fig. 5 shows the simulated diamond eye diagram of the 1-Gb/s pulse signals at the pre-amplifier input [point E of Fig. 2(a)] of the receiver chip after passing through a 10-cm PCB trace. The noise margin for V_{IH} and V_{IL} and the sensing (150–200 ps) and holding (800–850 ps) window of the pre-amplifier are defined here. In the null detecting range (between V_{term}–V_{m} and $V_{\mathrm{term}} + V_{\mathrm{m}}$ where $V_{\mathrm{term}} = 0.9$ V and $V_{\mathrm{m}} = 60$ mV), the pre-amplifier maintains the previous value with hysteresis characteristic. This provides an effective means of rejecting interference, which enables the receiver to be less sensitive to system noise with improved noise margin. The required minimum pulse amplitudes for the logical thresholds of the sensing operation, defined by V_{IH} (above $V_{\mathrm{term}} + V_{\mathrm{m}}$) and V_{IL} (below V_{term}–V_{m}), must be kept larger than the null detecting range.

Fig. 6 shows the simulated 2-Gb/s differential pulsed signaling using 0.8 pF C_C over a 10-cm FR4 PCB 2-drop bus from C to D as depicted in Fig. 2(a). When the transmitter chip 1 sends out 1-GHz binary data Din, it is converted to short pulses with V_p of about ± 300 mV and Tw of about 100 ps at point C/Cb. Then the transmitted pulses get attenuated and wider with V_p of about ± 150 mV and Tw of about 200 ps at point D/Db.

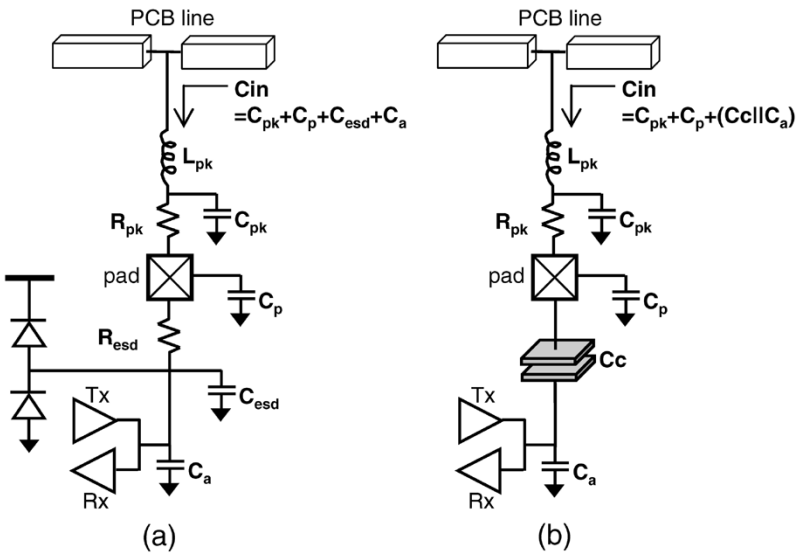


Fig. 7. Device loading model of (a) the conventional signaling bus, and (b) the pulsed signaling CCBI bus.

These are then recovered at the receiver chip 4. Since there is no need for coding/decoding of input/output signals or feedback schemes, the transmitter and receiver have no latency overhead compared to the conventional square wave signaling transceivers of high-speed DRAMs where low latency is very important for system performance.

IV. Signal Integrity

As the channel frequency, PCB trace length, and device loading count increase, conventional square wave voltage- or current-mode signaling on a shared multipoint bus using low-swing binary or even multilevel signals becomes exceedingly difficult [2], [14]. Also, the excessive increase in I/O signaling power, simultaneous switching noise (SSN), and package/board design complexity are becoming cost and reliability issues in battery-powered mobile systems and even in power-rich multichip systems consisting of over a few hundreds of high-speed I/O pins. Therefore, the signal integrity and the limited available bandwidth of a periodically loaded PCB channel are of increasing concern in high-speed buses. Here the signal integrity problem of a short distance (<30 cm) shared bus is mainly due to the impedance discontinuities created by the multiple device loadings along the channel [2], [14].

As shown in Fig. 7, this multiple device loading loss on a shared bus can be modeled with a series *RLC* network. For example, typical recent memory devices using chip scale packages have device input resistance Rin, inductance Lin, and capacitance Cin, as shown in Fig. 7(a). Here the input capacitance Cin $(=C_p + C_{\rm pk} + C_{\rm esd} + C_a)$ has a typical value of around 2 pF. It dominates the input reactive impedance Zin $(=\mathrm{Rin} + \mathrm{j}\omega\mathrm{Lin} + 1/\mathrm{j}\omega\mathrm{Cin})$ and attenuation up to a few gigahertz.

In the pulsed signaling transceiver on an ac coupled bus, as shown in Fig. 7(b), the device input capacitance using the same package is reduced to

$$\mathrm{Cin} = C_p + C_{\rm pk} + (C_C C_a)/(C_C + C_a) \approx 0.6\ \mathrm{pF} \quad (6)$$

where $C_C = 0.5$–0.8 pF, and $C_a = 0.25$ pF for the driver/receiver parasitic capacitance. This is only 30% of the conventional approach. Here, the Cin is primarily determined by the net package parasitic values plus the series combination of C_C and C_a. This is because C_C decouples the driver and receiver from the I/O pin. The ESD protection circuits, which usually add up to a few picofarads of capacitance to a device I/O, can be eliminated because the C_C blocks the dc current path. The elimination of ESD by covering the pad with oxide is well proven in proximity communication systems where a similar ac coupling approach is used [10], [11]. Therefore, multiple device loading losses from heavy capacitive loading effect are effectively decreased by moving added poles to much higher frequencies, resulting in less ISI on a shared bus as shown in Figs. 8 and 9.

Fig. 8 shows the simulated available channel bandwidth (3 dB cutoff frequency) of three types of double parallel terminated FR4 PCB microstrip lines used in the test board system as a function of the channel length: unloaded bus, 8-drop directly coupled bus, and 8-drop ac coupled bus. Although the unloaded 10-/20-/30-cm PCB traces have high cutoff frequencies of 6.1, 2.7, and 1.6 GHz, respectively, the channel bandwidth drops abruptly by the directly coupled device loadings. However, ac coupled buses achieve 43% to 127% higher 3 dB frequency than the directly coupled buses in the range of 10–30 cm. The simulation used the same WBGA package model for all cases. The package *RLC* parasitic values were extracted from the *S* parameter measurement in the frequency range of 300 KHz to 1 GHz by a vector network analyzer. The W-element RLGC transmission line model was calculated from the frequency response measurements and was used for SPICE simulation. The simulation assumes the device loading of a directly coupled bus has a total Cin of 1.8 pF, as shown in Fig. 7(a). It is composed of C_p (0.2 pF), $C_{\rm esd}$ (0.6 pF), driver/receiver C_a($0.6\,\mathrm{pF} + 0.2\,\mathrm{pF} = 0.8\,\mathrm{pF}$), and 10-$\Omega$ series resistance $R_{\rm esd}$. On the contrary, the device loading of an ac coupled bus using the same WBGA has an effective Cin of 0.6 pF, as shown in Fig. 7(b), with C_p (0.2 pF), C_C (0.8 pF), and C_a (0.25 pF).

Fig. 9(a) shows the channel transfer characteristics of the 10-/20-/30-cm directly coupled buses using this PCB trace with periodically mounted eight device loadings. It shows the 3 dB

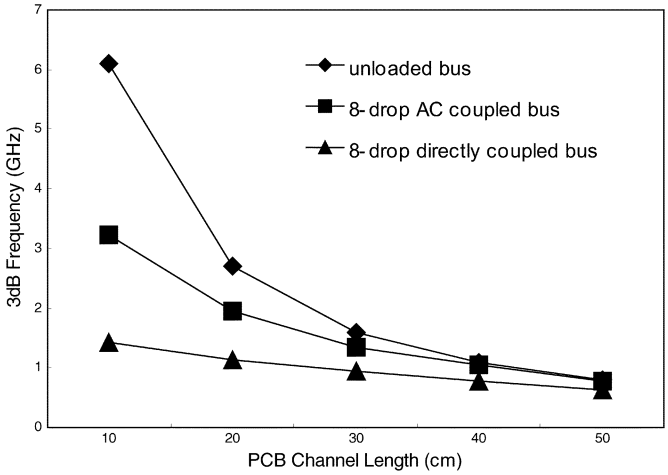


Fig. 8. Simulated available bus channel bandwidth.

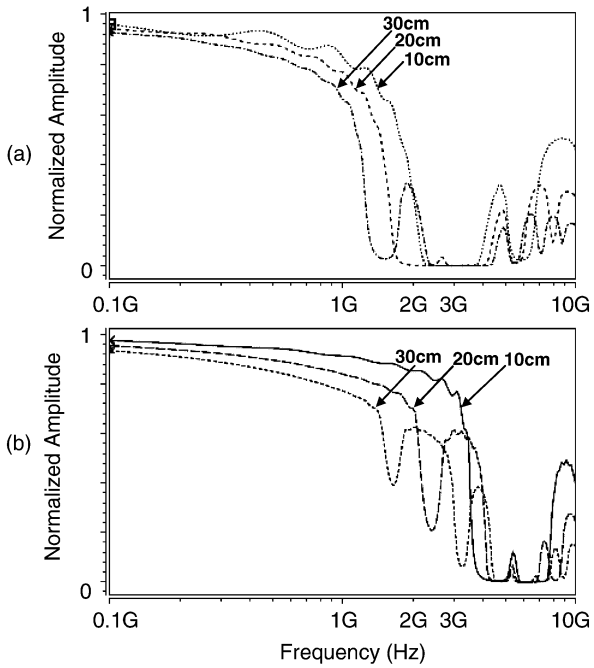


Fig. 9. Simulated channel transfer characteristics of the 8-drop (a) directly coupled bus and (b) ac coupled CCBI bus.

frequency of 1.42, 1.14, and 0.94 GHz, respectively. Fig. 9(b) shows the channel characteristics of the 10-/20-/30-cm fully ac coupled buses using the same PCB trace with the same number of loadings. The simulation results indicate a considerably improved 3 dB frequency of 3.22, 1.95, and 1.35 GHz, respectively. This extended available bandwidth is because the input impedance Zin of the pulsed signaling transceiver is much larger than the channel characteristic impedance Z_o. Also, the input capacitance Cin of the pulsed signaling transceiver is much less than that of the directly coupled bus transceivers. Therefore, the simulation results demonstrate that the fully ac coupled bus is much less sensitive to the multiple device loading losses. Moreover, the high pass transmission characteristic of an ac coupled bus rejects the low frequency noise in the transceiver system. The smaller I/O signaling power, which is discussed in Section V, results in reduced simultaneous switching noise generation on the power and ground planes. Differential signaling inherently minimizes the effect of common-mode noise disturbances such as cross talk and power supply noise. The use of hysteresis in the receiver circuit also improves the noise immunity by rejecting interference noise. Consequently, although PCB channel skin effect and dielectric losses still exist, the signal integrity problems of a fully ac coupled bus using differential pulsed signaling become much less severe than conventional directly coupled buses using square wave signaling. Therefore, this less noisy CCBI channel with high signal-to-noise ratio makes it possible to send short pulse signal through a PCB trace with less energy transmission.

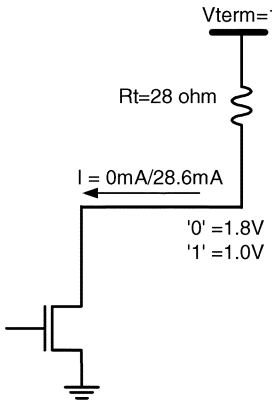
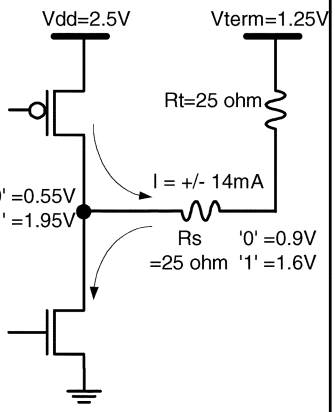
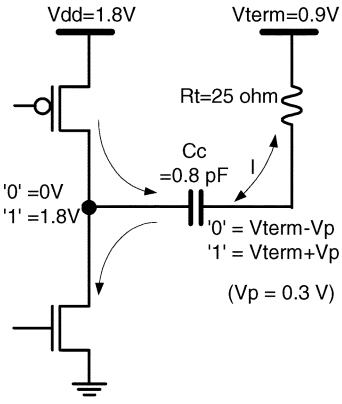
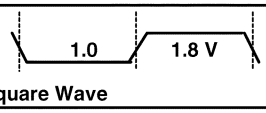
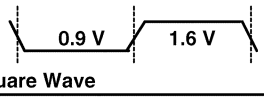
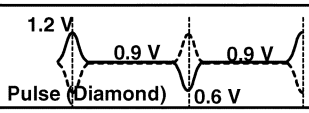
V. Channel Power Dissipation

This paper focuses on power dissipation of parallel high-speed multipoint buses such as memory interfaces. Table I compares the I/O signaling power of the most recent memory interfaces using a directly coupled multipoint bus topology [15]–[17] [i.e., Rambus Signaling Levels (RSL) for 1.2-Gb/s/pin Rambus DRAM (RDRAM) and Stub Series Terminated Logic (SSTL) for 800-Mb/s/pin DDR SDRAM] and the proposed 1-Gb/s/pair pulsed signaling. Currently in the market, the RDRAM and DDR SDRAM are now providing 1066 Mb/s/pin and 667 Mb/s/pin, respectively. We compare however with their future highest data rate. The DDR-I and DDR-II use different power supply of 2.5 and 1.8 V, respectively, but both use basically the same SSTL signaling scheme except for the use of an on-die termination in DDR-II [17]. In Table I, we focus on the power dissipation of the final stage output driver and the channel termination. We assume the signal swing of the RSL and SSTL are 0.8 and 0.7 V, respectively. To simplify the comparison, this table does not consider the other sources of signaling power consumption: pre-driver power (the power required to drive the output driver) and receiver power. The pre-driver of the conventional schemes usually consumes very large power to drive the heavy final-stage output driver with a fast slew rate. The receiver power is usually much smaller than the driver power in memory interfaces.

The 1.2-Gb/s RSL dissipates 28.6 mW (1 V $\times$ 28.6 mA) for the open drain current-mode output driver and 22.9 mW $((0.8\ \mathrm{V})^2/28\Omega)$ for the termination with a 28-Ω resistor for a 0.8-V channel swing by sinking 28.6 mA per line. The total average power is 25.75 mW for data patterns with a balanced stream of 1's and 0's, which means the worst-case power dissipation could be doubled to 51.5 mW. The SSTL consumes 7.7 mW (0.55 V $\times$ 14 mA) for the push-pull type output driver, 4.9 mW $((0.35\ \mathrm{V})^2/25\ \Omega)$ for the channel termination with two parallel 50-Ω resistors (effective $R_t = 25\,\Omega$), and 4.9 mW $((0.35\ \mathrm{V})^2/25\ \Omega)$ for the series termination with a 25-Ω resistor for a 0.7-V swing by sinking 14 mA. The total power dissipation of SSTL is 17.5 mW for a data rate of 800 Mb/s.

In pulsed signaling CCBI, the single output driver dissipates a maximum dynamic power of 1.3 mW ($C_C V dd^2 f = 0.8$ pF $(1.8\,\mathrm{V})^2/2$ ns) to drive the C_C of 0.8 pF with a rail-to-rail swing. Since the channel has no dc current consumption, the channel termination power for the two parallel 50-Ω resistors is only 0.15 mW. Thus, the total power dissipation is reduced to only 2.9 mW/pair at 500 MHz for a data rate of 1 Gb/s/pair. By calculating the energy per bit (or the power for a specific data rate),

TABLE I
I/O SIGNALING POWER AND ENERGY EFFICIENCY OF RSL, SSTL, AND THIS WORK

	RSL (1.2 Gb/s)	SSTL (800 Mb/s)	This work (1 Gb/s)
Output Driver			
Type	Open Drain	Push Pull	Push Pull
Termination	Single Parallel	Double Parallel	Double Parallel
I/O Frequency	600MHz (1.2Gb/s)	400MHz (800Mb/s)	500MHz (1Gb/s)
Signal Swing			
Driver Power	28.6 mW	7.7 mW	1.3 mW
Termination Power	22.9 mW	9.8 mW	0.15 mW
Total Power	51.5 mW (worst) 51.5 mW/2=25.75 mW (avg.)	17.5 mW	1.45 mWx2=2.9 mW (diff.)
Energy Efficiency	43 pJ/bit (worst) 21.5 pJ/bit (avg.)	21.9 pJ/bit	2.9 pJ/bit

the energy efficiency of these bus I/O schemes can be compared. The energy to transfer one bit data can be defined as

$$\text{Energy/bit} = \text{Power/data rate}. \tag{7}$$

The SSTL and RSL dissipate 21.9 pJ/bit and 21.5 pJ/bit, respectively. However, pulsed signaling consumes only a maximum of 2.9 pJ/bit. This shows that pulsed signaling CCBI is 7.5 times more energy efficient than the above most recent memory interface schemes.

VI. MEASUREMENT RESULTS

The test transceiver chip in Fig. 10 was fabricated in a 0.10-μm CMOS DRAM technology and packaged in a WBGA. The transceiver active area is 330×85 μm^2 and each 0.8-pF on-chip MIM C_C occupies an area of 110×110 μm^2. We intentionally kept the ESD structures ($C_{\text{esd}} = 0.6$ pF), located in between the pad and C_C, for more heavy capacitive loading effects in this test PC board. Therefore, a capacitance of $C_C1 = C_C2 = 0.8$ pF was chosen. If we remove the ESD circuits, the C_C can be reduced to 0.5 pF. Also, the capacitor area can be reduced by using thin dielectric layers or high dielectric constant materials or by forming the capacitor under the bonding pad. Fig. 11 shows the measurement setup for a 2-drop 10-cm long (Tx to Rx) standard FR4 PC board with double parallel terminated 50-Ω differential microstrip lines, consisting of two WBGA packages are flip-chip mounted. In Fig. 12, the 1-Gb/s single-ended pulse signals are measured on the backside of this test board. Fig. 12(a) shows the pulses at the transmitter side [point C of Fig. 2(a)] with a V_p of about 200 mV. Fig. 12(b) shows the transmitted pulses with a V_p of about 100 mV and a Tw of about 200 ps at the receiver side (point D) after a 10-cm flight at 500-MHz operating frequency. The measured pulses are in good correspondence with the simulated 2-Gb/s pulsed signaling of Fig. 6. This also shows the possibility of increasing the data rate up to 5 Gb/s. In spite

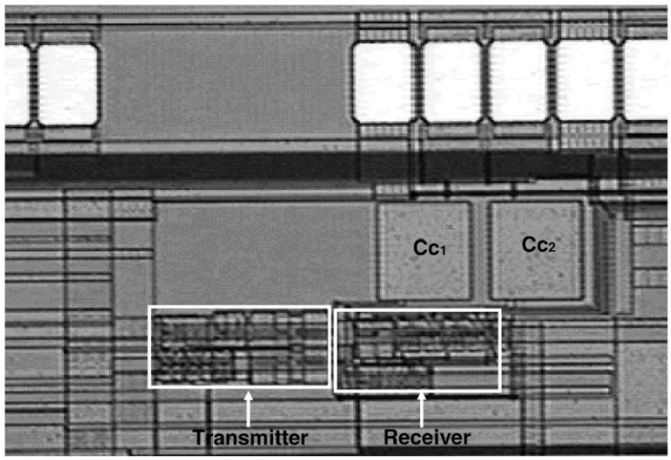


Fig. 10. Transceiver chip microphotograph.

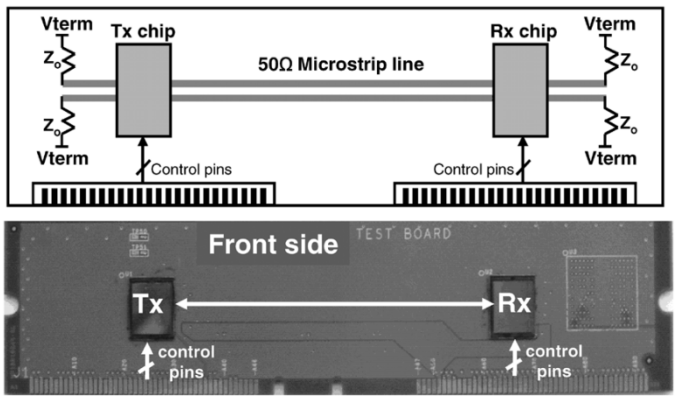


Fig. 11. Measurement test PC board.

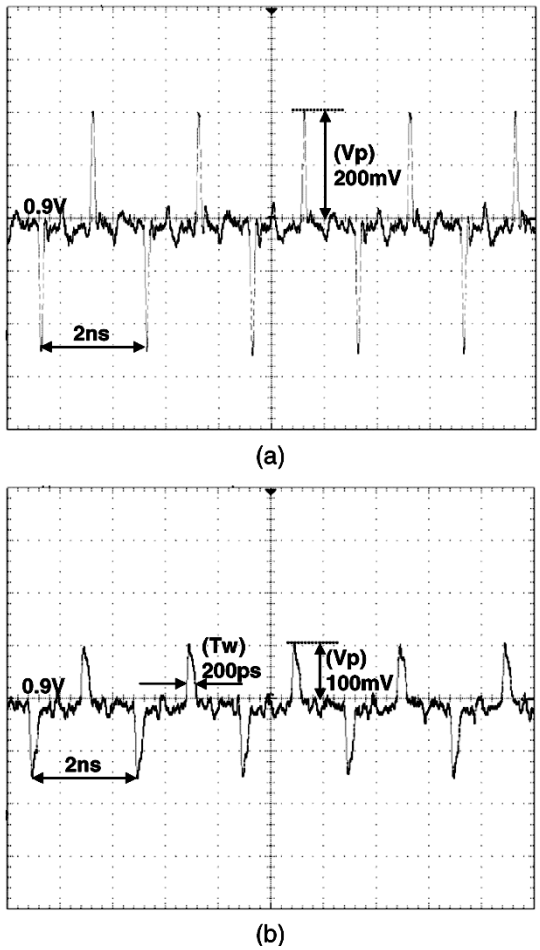


Fig. 12. Measured 1-Gb/s pulse signals on the test PC board (a) at the transmitter side [point C of Fig. 2(a)] and (b) at the receiver side (point D) after 10-cm flight.

of the existence of the ESD protection overhead and the dispersions of the pulses delivered to the receiver chip through the PCB channel, the incoming pulses are well recovered without errors for 24 hours. Table II summarizes the performance of the CCBI transceiver chipset.

TABLE II
PERFORMANCE SUMMARY

Supply Voltage	1.8V
Technology	0.10-μm CMOS DRAM process
Data Rate	1.0Gb/s/pair (at 500MHz)
Power Dissipation (Termination)	0.3 mW/pair
Power Dissipation (Transmitter)	2.6 mW (differential driver)
Power Dissipation (Receiver)	2.7 mW (static pre-amplifier)
Active Transceiver (Tx+Rx) Area	330×85 μm^2

VII. CONCLUSION

A 1-Gb/s pulsed signaling I/O transceiver on a fully ac coupled multipoint bus has been designed, fabricated, and tested in a 0.10-μm 1.8-V CMOS DRAM technology. By comparing the power per data rate, this CCBI signaling technique consumes 7.5 times less energy/bit than the most recent memory bus interfaces. The differential pulsed signaling transceiver design and the fully ac coupled bus topology demonstrates the methods of improving signal integrity with less signaling power dissipation. The transmitter and channel power is reduced by using a diamond data eye, which has no dc power component unlike the conventional square wave signaling. By using on-chip capacitive coupling, the fully ac coupled multipoint bus reduces the impedance discontinuity and the ISI and therefore increases the available channel bandwidth. Pulsed signaling employing these techniques is suitable for use in high-speed board-level chip-to-chip communications to achieve low latency, low power, and high signal integrity.

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